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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 043290.P3955D Total Pages 5

First Named Inventor or Application Identifier Ebrahim Andideh et al.

Express Mail Label No. EL388636027US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 28)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 5)

4. X Oath or Declaration (Total Pages 5)
   a. ___ Newly Executed (Original or Copy)
   b. X Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. X Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ________ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ________ Computer Readable Copy
b. ________ Paper Copy (identical to computer copy)
c. ________ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
____ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. X a. Information Disclosure Statement (IDS)/PTO-1449
X b. Copies of IDS Citations
12. X Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. X Other: postcard with Express Mail label

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation X Divisional ____ Continuation-in-part (CIP)
of prior application No: 08/997,293 Filed December 23, 1997

18. **Correspondence Address**
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Attorney's Docket No.: 042390.P3955D

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)		
Ebrahim Andideh et al.	)	Examiner:	Not yet assigned
Serial No: Not yet assigned	)	Art Unit:	Not yet assigned
Filed: November 8, 1999	)		
For: Polish Pad with Non-Uniform Groove Depth to Improve Wafer Polish Rate Uniformity	)		

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to an examination of the above-identified application, and prior to calculating the filing fee of the enclosed divisional application, please enter the following amendments.

IN THE CLAIMS:

Please cancel claims 1-26, without prejudice as drawn to a non-elected invention. Claims 27-53 remain in the application and are drawn to an apparatus, classified in class 156, subclass 345.

REMARKS

Reconsideration of this application in view of the foregoing amendments and the following remarks is respectfully requested.

Applicants respectfully requests consideration of this application in view of the foregoing amendments. This divisional application is being filed in response to an election requirement mailed on April 23, 1999, for parent case serial no. 08/997,293 filed on

December 23, 1997. Claims 27-53 remain in this divisional application. Please enter the amendment before calculating the filing fee of the enclosed divisional application.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Darren J. Milliken at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 11/8, 1999

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November 8, 1999
(Date signed)

UNITED STATES PATENT APPLICATION

FOR

POLISH PAD WITH NON-UNIFORM GROOVE DEPTH TO IMPROVE WAFER POLISH RATE UNIFORMITY

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POLISH PAD WITH NON-UNIFORM GROOVE DEPTH TO IMPROVE WAFER POLISH RATE UNIFORMITY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of semiconductor processing, and more specifically, to polishing methods and polishing pads for planarizing semiconductor materials in the fabrication of semiconductor devices.

2. Background Information

Semiconductor devices manufactured today generally rely upon an elaborate system of semiconductor device layers, patterns, and interconnects. The techniques for forming such various device layers, patterns, and interconnects are extremely sophisticated and are well understood by practitioners in the art. During fabrication, however, these varying device layers, patterns, and interconnects often create non-planar wafer topographies. Such non-planar wafer topographies cause difficulties when forming subsequent device layers, insulating layers, levels of interconnects, etc.

Some problems associated with non-planar topographies, for example, are the interference and scattering of radiation by the non-planar topography when performing photolithographic process steps. This makes it particularly difficult to print patterns with high resolution. Another problem with non-planar topographies is in depositing metal layers or lines.

Uneven topographies, or step-heights as they are often called, may cause thinning of the metal line/layer at points where the topography transitions from a high point to a low point, and vice versa. Such thinning of the metal layers may cause open circuits to be formed in the device or may cause the device to suffer reliability problems.

To combat these problems, various techniques have been developed in an attempt to planarize the topography of the wafer surface prior to performing additional processing steps. One approach employs abrasive polishing, for example chemical mechanical polishing (CMP), to remove the high points along the upper surface. According to this method, the wafer is placed on a table and is polished with a pad that has been coated with an abrasive material (i.e. slurry). Both the wafer and the table are rotated relative to each other to remove the high portions of the wafer topography. This abrasive polishing process continues until the upper surface of the wafer is largely planarized.

One problem with polishing to planarize the topography is that the polishing rates can become unstable and/or uneven across the surface of the wafer. For example, the profile of the topography in certain areas of the wafer may affect the polishing rate in that area. Figure 1 illustrates a simple example of the polishing rate profile of a wafer 100. As is illustrated in Figure 1, the polishing rate at the edges 110 of wafer 100 is slower than the polishing rate toward the center 120 of wafer 100 (i.e., edge slow). The difference in polish rates across the wafer may cause the topography of the

wafer to be uneven after polishing. For example, the polishing rate profile of Figure 1 may cause the wafer topography to have low points in the center of the wafer and high points around the edges of the wafer, rather than a flat or planar surface as is desired.

It is desired to have an even polish rate profile across the wafer surface in order to improve the planarity of the polishing process. As illustrated in Figure 1, an ideal polish rate profile is illustrated in Figure 1 by dashed line 150. In order to arrive at the ideal polish rate profile 150, what is needed is method to increase the polish rate at the edges of the wafer 110, and decrease the polish rate at the center of the wafer 120. The ideal polish rate profile 150 will improve the surface planarity of the polishing process.

Figures 2 and 3 also illustrate examples wherein the polishing rates are uneven/unstable across the surface of a wafer. Figure 2, illustrates the opposite effect of Figure 1, wherein the polishing rate at the edges 210 of wafer 200 is faster than the polishing rate toward the center 220 of wafer 200 (i.e., center slow). Thus in Figure 2, what is needed is a method to decrease the polish rate at the edges of the wafer 210, and increase the polish rate at the center of the wafer 220, in order to obtain the ideal polish rate profile 250. Figure 3, illustrates a worst case scenario wherein the polishing rate varies randomly across the entire wafer surface. Thus in Figure 3, what is needed is a method to decrease the polish rate in the areas of the wafer 300 where the polish rate is high, and increase the polish rate in the areas of the wafer

300 where the polish rate is low, in order to obtain the ideal polish rate profile 350.

Thus, what is needed is a method to increase the polish rate in the areas of a semiconductor wafer that the polish rate is low and/or decrease the polish rate in the areas of a semiconductor wafer that the polish rate is high in order to improve the planarization process of the semiconductor wafer.

SUMMARY OF THE INVENTION

The present invention describes a method for creating a differential polish rate across a semiconductor wafer . One embodiment of the present invention determines the profile of the semiconductor wafer by locating the high points and low points of the wafer profile. A grooved polish pad is provided and then the groove depth of the polish pad is adjusted by increasing the groove depth in the areas of the polish pad that correspond to the high points of said wafer profile. The semiconductor wafer is then polished with the polish pad.

Additional features and benefits of the present invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which:

Figure 1 illustrates an edge slow polish rate profile of a semiconductor wafer.

Figure 2 illustrates a center slow polish rate profile of a semiconductor wafer.

Figure 3 illustrates a random polish rate profile of a semiconductor wafer.

Figure 4a illustrates a cross-sectional view of a polish pad having v-shaped grooves.

Figure 4b illustrates a cross-sectional view of a polish pad having u-shaped grooves.

Figure 4c illustrates a cross-sectional view of a polish pad having one-sided triangle grooves.

Figure 5a illustrates a cross-sectional view of a polish pad having v-shaped grooves according to one embodiment of the present invention and the polish rate profile of Figure 1.

Figure 5b illustrates a cross-sectional view of a polish pad having u-shaped grooves according to another embodiment of the present invention and the polish rate profile of Figure 1.

Figure 6 illustrates a cross-sectional view of a polish pad having u-shaped grooves according to still another embodiment of the present invention and the polish rate profile of Figure 2.

Figure 7 illustrates a cross-sectional view of a polish pad having u-shaped grooves according to yet another embodiment of the present invention and the polish rate profile of Figure 3.

DETAILED DESCRIPTION

A(n) Polish Pad With Non-Uniform Groove Depth To Improve Wafer Polish Rate Uniformity is disclosed. In the following description, numerous specific details are set forth such as specific materials, patterns, dimensions, etc. in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the present invention.

The present invention describes a method for improving the surface planarity during the fabrication of semiconductor device layers. The multi-layered structure of current semiconductor devices often leads to non-planar surfaces that can cause problems during the fabrication of subsequent device layers. One method developed to help solve the problem of non-planar wafer topographies is the use of chemical mechanical polishing (CMP) to planarize the wafer surface.

There are many factors that play a part in the planarization process. For chemical mechanical polishing, some of these factors include: the rotation rates of the polishing pad and wafer, the wafer topography or profile (i.e. the high points and low points on the wafer surface), the pressure with which the pad and wafer are put in contact, the material making up the polish pad, the slurry being used, the material being polished/planarized/removed, etc. All of these factors are important to the

planarization process, however, even if all of these factors are optimized some planarization problems may still exist.

The present invention may be used singly or in combination with any of the above mentioned factors and optimization parameters to improve the planarization process. One embodiment of the present invention determines the profile or topography of the wafer. In other words, it is determined where the high points and low points are on the wafer surface. It should be obvious to one with ordinary skill in the art that well know methods for determining wafer topography may be used and are therefore not discussed in detail herein.

Typically, a polish pad will contain grooves such as those illustrated in Figures 4a-c. Figure 4a illustrates a polish pad having v-shape grooves therein. Figure 4b illustrates a polish pad having u-shape grooves therein. Figure 4c illustrates a polish pad having single-sided triangle grooves therein. Although, Figures 4a-c illustrate only a single shape of groove per polish pad, it should be noted that different groove shapes and/or a combination of groove shapes may be used on a polish pad.

Generally, the grooves are cut into the polish pad during manufacture of the polish pad and are usually uniformly spaced across the diameter of the polish pad. Additionally, the groove depth and groove width are uniform across the polish pad surface. However, such uniform groove density, groove width, and groove depth may cause non-uniform polish

rates across the wafer surface such as those illustrated in Figures 1-3, edge slow, center slow, and random, respectively.

The present invention improves the planarization process by adjusting and/or changing the grooves which are in the polishing pad. Groove shape, groove depth, groove width, and groove density all play a part in the planarization process. Changing the groove shape, groove depth, groove width, and/or groove density, either singly or in combination, can affect the polishing rate of the wafer. As such, changing the groove shape, groove depth, groove width, and/or groove density, either singly or in combination, also affects the polish rate profile of the wafer.

By changing the grooves in the areas of the polish pad that correspond to the areas of the wafer where the high points and low points of the wafer topography and/or the areas where the polish rate profile is either high or low, the polish rate may be stabilized. Stabilizing the polish rate will in turn improve planarization. By increasing the groove depth, width, and/or density the polish rate is increased which will more effectively remove the high points in the wafer topography and/or stabilize the polish rate in areas of the wafer where the polish rate would have been too low. For example in Figure 1 that illustrates edge slow, the groove depth, width, and/or density would be increased in the areas of the polish pad that correspond to the edges of the semiconductor wafer in order to increase the polish rate so that the desirable polish profile 150 may be achieved.

By decreasing the groove depth, width, and/or density the polish rate is decreased which will remove less of the topography near the low points and/or stabilize the polish rate in areas of the wafer where the polish rate would have been too high and otherwise would have removed too much of the topography. For example, in Figure 2 that illustrates center slow, the groove depth, width, and/or density would be decreased in the areas of the polish pad that correspond to the center of the semiconductor wafer in order to decrease the polish rate at the center of the wafer so that the desirable polish profile 250 may be achieved. Similar adjustments may be made in Figure 3 that illustrates a random wafer profile in order to achieve the desirable polish rate profile 350.

It should be noted and it will be obvious to one with ordinary skill in the art given this description that the grooves may be changed in any number of combinations. For example, in Figure 1 that illustrates edge slow, the groove depth, width. and/or density may be increased at the edges of the wafer and may be decreased at the center of the wafer. Depending upon the result desired by the user, just the groove depth , or just the groove width, or just the groove density may be increased or decreased in some areas. The user may also determine that it would be more beneficial to adjust groove depth and groove width, or groove depth and groove density, or groove width and groove density, or all three: groove depth, width, and density in some areas to obtain the desired result. Thus, the grooves may be

adjusted in many various combinations in order to achieve the optimum polish rate profile desired by a particular user.

Figure 5a illustrates a cross-sectional view of a polish pad having v-shaped grooves according to one embodiment of the present invention and the polish rate profile of Figure 1. In order to achieve the desired polish rate profile 150 the groove width and groove depth of the grooves in the center of the polish pad of Figure 5a are increased in order to increase the polish rate at the center of the wafer. Figure 5b illustrates a cross-sectional view of a polish pad having u-shaped grooves according to another embodiment of the present invention and the polish rate profile of Figure 1. Similar to Figure 5a, the grooves of the polish pad in Figure 5b increase in depth and density in order to increase the polish rate at the center of the wafer. The polish pads of Figures 5a and 5b correspond to a wafer profile wherein the wafer has low points at the edge of the wafer and high points at the center of the wafer. Thus, where the wafer profile has high points in the center of the wafer and the polish rate would ordinarily be slow the present invention increases the groove depth, width, and/or density in order to increase the polish rate and remove the high points of the topography to achieve the desired wafer profile 150.

Figure 6 illustrates a cross-sectional view of a polish pad having u-shaped grooves according to still another embodiment of the present invention and the polish rate profile of Figure 2. The polish pad of Figure 6 corresponds to a wafer profile wherein the wafer has high points at the edge

of the wafer and low points at the center of the wafer. As illustrated in Figure 6 the depth and width of the grooves at the edges are increased in order to increase the polish rate at the edges of the wafer. Also, as illustrated in Figure 6 the depth and width of the grooves at the center of the polish pad are decreased in order to reduce (or decrease) the polish rate at the center of the wafer. Thus, the polish pad of Figure 6 may be used to increase the polish rate at the edge of the wafer and decrease the polish rate in the center of the wafer in order to achieve the desired polish rate profile 250 illustrated in Figure 2.

Figure 7 illustrates a cross-sectional view of a polish pad having u-shaped grooves according to yet another embodiment of the present invention and the polish rate profile of Figure 3. The polish pad of Figure 7 corresponds to a wafer profile wherein the wafer has random high points and low points. As illustrated in Figure 7 the depth, width, and density of the grooves are increased in the areas of the polish pad corresponding to high points of the wafer profile in Figure 3. Also, as illustrated in Figure 7 the depth, width, and density of the grooves are decreased in the areas of the polish pad corresponding to low points of the wafer profile in Figure 3. Thus, the polish pad of Figure 7 may be used to increase the polish rate in areas of the wafer wherein the high points would otherwise cause the polish rate to be low and decrease the polish rate in areas of the wafer wherein the low points would otherwise cause the polish rate to be too high in order to achieve the desired polish rate profile 350 illustrated in Figure 3.

It should be noted that the grooves of the polish pad should be adjusted while keeping in mind the parameters of the particular polish pad so not to degrade the usefulness of the polish pad. For example, the depth of the grooves should not be increase to the point where the polish pad becomes weak or brittle. As another example, the width of the grooves should not be increased to be so large as not to be effective or cover too large an area on the polish pad. Likewise, the density of the grooves should not be increased beyond the point where the portions of the polish pad that separate the grooves are too thin or brittle and may break.

In one embodiment of the present invention the groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness. In another embodiment of the present invention the groove width is adjusted within the range of approximately 1 - 100 mils. In yet another embodiment of the present invention the groove density is adjusted within the range of approximately 2 - 50 grooves/inch. It will be obvious to one with ordinary skill in the art that such parameters may be dependent upon the strength, durability, surface area, pad thickness, material, and etc. that make up the polish pad.

It should be noted that deeper and/or wider and/or more dense grooves improve slurry transport and distributes more slurry to the areas where a higher polish rate is desired. It should also be noted that wider grooves and/or more dense grooves increase the pressure in the areas where a higher polish rate is desired. By changing the groove depth, width, and/or

density the present invention distributes more slurry and/or increases the pressure of the polish pad in the areas where a higher polishing rate is desired in order to achieve the desired polish profiles, for example, polish profiles 150, 250, and 350 illustrated in Figures 1, 2, and 3, respectively.

Thus, Polish Pad With Non-Uniform Groove Depth To Improve Wafer Polish Rate Uniformity has been described. Although specific embodiments, including specific equipment, patterns, methods, and materials have been described, various modifications to the disclosed embodiments will be apparent to one of ordinary skill in the art upon reading this disclosure. Therefore, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention and that this invention is not limited to the specific embodiments shown and described.

CLAIMS

What is claimed is:

1. A method for creating a differential polish rate across a wafer comprising:

determining the profile of said wafer, said wafer profile having high points and low points;

providing a polish pad having a plurality of grooves;

adjusting the groove depth of said polish pad, wherein said groove depth is increased in the areas of said polish pad that correspond to the high points of said wafer profile; and

polishing said wafer with said polish pad.

2. The method as described in claim 2 further comprising the step of:

adjusting the groove width of said polish pad, wherein said groove width is increased in the areas of said polish pad that correspond to the high points of said wafer profile.

3. The method as described in claim 2 further comprising the step of:

adjusting the groove density of said polish pad, wherein said groove density is increased in the areas of said polish pad that correspond to the high points of said wafer profile.

4. The method as described in claim 1 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

5. The method as described in claim 1 wherein said groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness.

6. The method as described in claim 2 wherein said groove width is adjusted within the range of approximately 1 - 100 mils.

7. The method as described in claim 3 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

8. A method for creating a differential polish rate across a wafer comprising:

determining the profile of said wafer, said wafer profile having high points and low points;

providing a polish pad having a plurality of grooves;

adjusting the groove width of said polish pad, wherein said groove width is increased in the areas of said polish pad that correspond to the high points of said wafer profile; and

polishing said wafer with said polish pad.

9. The method as described in claim 8 further comprising the step of: adjusting the groove depth of said polish pad, wherein said groove depth is increased in the areas of said polish pad that correspond to the high points of said wafer profile.

10. The method as described in claim 8 further comprising the step of: adjusting the groove density of said polish pad, wherein said groove density is increased in the areas of said polish pad that correspond to the high points of said wafer profile.

11. The method as described in claim 8 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

12. The method as described in claim 8 wherein said groove width is adjusted within the range of approximately 1 - 90% of the pad thickness.

13. The method as described in claim 9 wherein said groove depth is adjusted within the range of approximately 0.01 - 50 mils.

14. The method as described in claim 10 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

15. A method for creating a differential polish rate across a wafer comprising:

determining the profile of said wafer, said wafer profile having high points and low points;

providing a polish pad having a plurality of grooves;

increasing the polish rate of said polish pad in the areas of said polish pad that correspond to the high points of said wafer profile; and

polishing said wafer with said polish pad.

16. The method as described in claim 15 wherein said step of increasing the polish rate comprises increasing the groove depth of said grooves in the areas of said polish pad that correspond to the high points of said wafer profile.

17. The method as described in claim 15 wherein said step of increasing the polish rate comprises increasing the groove width of said grooves in the areas of said polish pad that correspond to the high points of said wafer profile.

18. The method as described in claim 15 wherein said step of increasing the polish rate comprises increasing the groove density of said grooves in the areas of said polish pad that correspond to the high points of said wafer profile.

19. The method as described in claim 15 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

20. The method as described in claim 16 wherein said groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness.

21. The method as described in claim 17 wherein said groove width is adjusted within the range of approximately 1 - 100 mils.

22. The method as described in claim 18 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

23. The method of claim 15 further comprising the step of:

decreasing the polish rate of said polish pad in the areas of said polish pad that correspond to the low points of said wafer profile.

24. The method as described in claim 23 wherein said step of decreasing the polish rate comprises decreasing the groove depth of said grooves in the areas of said polish pad that correspond to the low points of said wafer profile.

25. The method as described in claim 23 wherein said step of decreasing the polish rate comprises decreasing the groove width of said grooves in the areas of said polish pad that correspond to the low points of said wafer profile.

26. The method as described in claim 23 wherein said step of decreasing the polish rate comprises decreasing the groove density of said grooves in the areas of said polish pad that correspond to the low points of said wafer profile.

27. A polish pad for creating a differential polish rate across a wafer comprising:

said polish pad having a plurality of grooves;

said grooves having an increased depth in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased depth in areas that correspond to low points on the surface of said wafer.

28. The polish pad as described in claim 27 further comprising:

said grooves having an increased width in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased width in areas that correspond to low points on the surface of said wafer.

29. The polish pad as described in claim 27 further comprising:

said grooves having an increased density in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased density in areas that correspond to low points on the surface of said wafer.

30. The polish pad as described in claim 27 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

31. The polish pad as described in claim 27 wherein said groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness.

32. The polish pad as described in claim 28 wherein said groove width is adjusted within the range of approximately 1 - 100 mils.

33. The polish pad as described in claim 29 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

34. A polish pad for creating a differential polish rate across a wafer comprising:

said polish pad having a plurality of grooves;

said grooves having an increased width in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased width in areas that correspond to low points on the surface of said wafer.

35. The polish pad as described in claim 34 further comprising:

said grooves having an increased depth in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased depth in areas that correspond to low points on the surface of said wafer.

36. The polish pad as described in claim 34 further comprising:

said grooves having an increased density in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased density in areas that correspond to low points on the surface of said wafer.

37. The polish pad as described in claim 34 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

38. The polish pad as described in claim 34 wherein said groove width is adjusted within the range of approximately 1 - 90% of the pad thickness.

39. The polish pad as described in claim 35 wherein said groove depth is adjusted within the range of approximately 0.01 - 50 mils.

40. The polish pad as described in claim 36 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

41. A polish pad for creating a differential polish rate across a wafer comprising:

said polish pad having a plurality of grooves;

said grooves having an increased density in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased density in areas that correspond to low points on the surface of said wafer.

42. The polish pad as described in claim 41 further comprising:

said grooves having an increased width in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased width in areas that correspond to low points on the surface of said wafer.

43. The polish pad as described in claim 41 further comprising:

said grooves having an increased depth in areas that correspond to high points on the surface of said wafer; and

said grooves having a decreased depth in areas that correspond to low points on the surface of said wafer.

44. The polish pad as described in claim 41 wherein said plurality of grooves have a shape consisting of: a v-shape, a u-shape, a one-sided-triangle, or a combination thereof.

45. The polish pad as described in claim 41 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

46. The polish pad as described in claim 42 wherein said groove width is adjusted within the range of approximately 1 - 100 mils.

47. The polish pad as described in claim 43 wherein said groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness.

48. A polish pad comprising:

a plurality of groves, said plurality of grooves having varying groove densities.

49. The polish pad as described in claim 48 wherein said groove density is adjusted within the range of approximately 2 - 50 grooves/inch.

50. A polish pad comprising:

a plurality of grooves, said plurality of grooves having varying groove depths.

51. The polish pad as described in claim 50 wherein said groove depth is adjusted within the range of approximately 1 - 90% of the pad thickness.

52. A polish pad comprising:

a plurality of grooves, said plurality of grooves having varying groove widths.

53. The polish pad as described in claim 52 wherein said groove width is adjusted within the range of approximately 1 - 100 mils.

ABSTRACT OF THE DISCLOSURE

The present invention describes a method for creating a differential polish rate across a semiconductor wafer . The profile or topography of the semiconductor wafer is determined by locating the high points and low points of the wafer profile. The groove pattern of a polish pad is then adjusted to optimize the polish rate with respect to the particular wafer profile. By increasing the groove depth, width, and/or density of the groove pattern of the polish pad the polish rate may be increased in the areas that correspond to the high points of the wafer profile. By decreasing the groove depth, width, and/or density of the groove pattern of the polish pad the polish rate may be decreased in the areas that correspond to the low points of the wafer profile. A combination of these effects may be desirable in order to stabilize the polish rate across the wafer surface in order to improve the planarization of the polishing process.

Polish Rate Profile Across a Wafer
(Edge Slow)

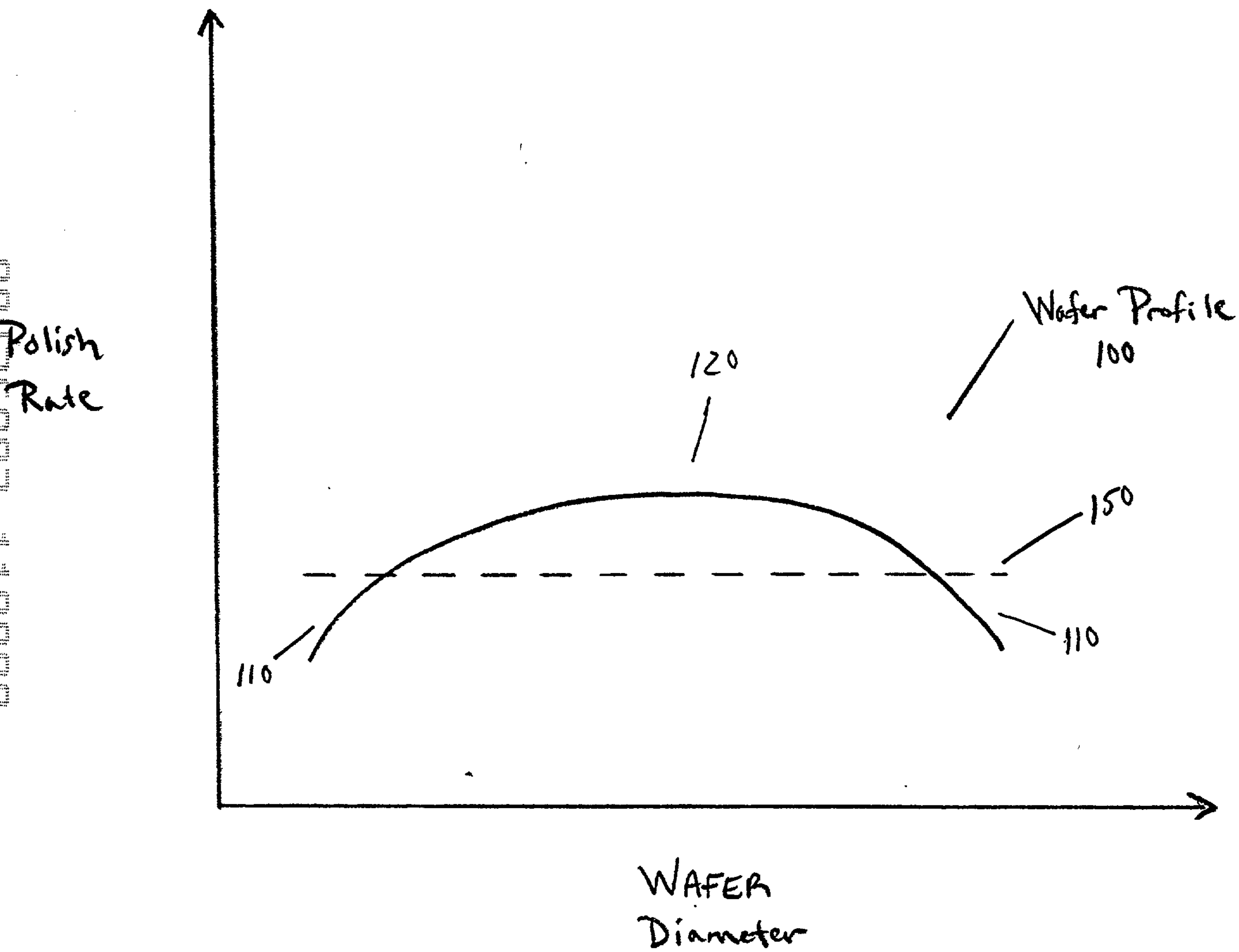

FIGURE 1

Polish Rate Profile Across a Wafer
(Center Slow)

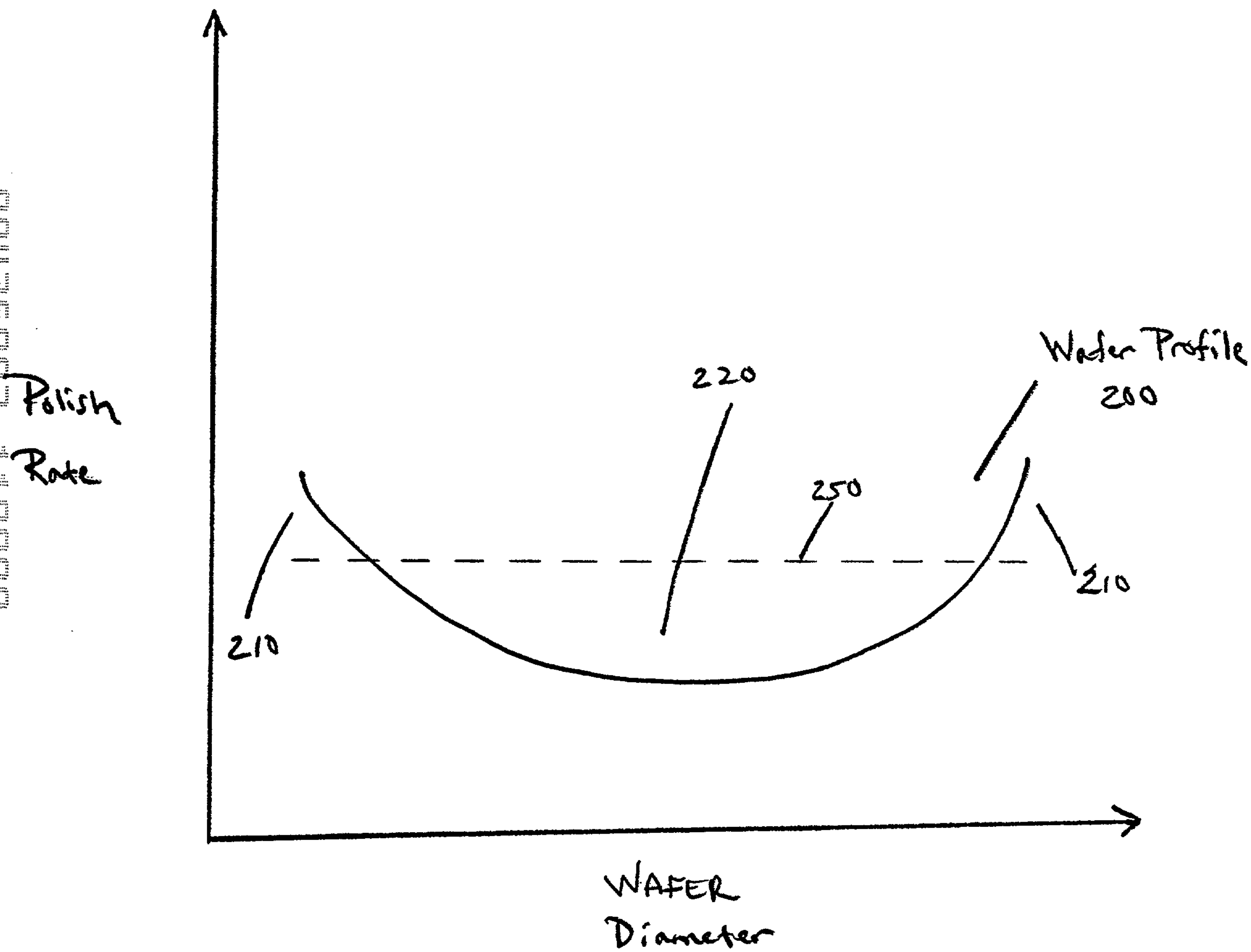

FIGURE 2

Polish Rate Profile Across a Wafer
(Random)

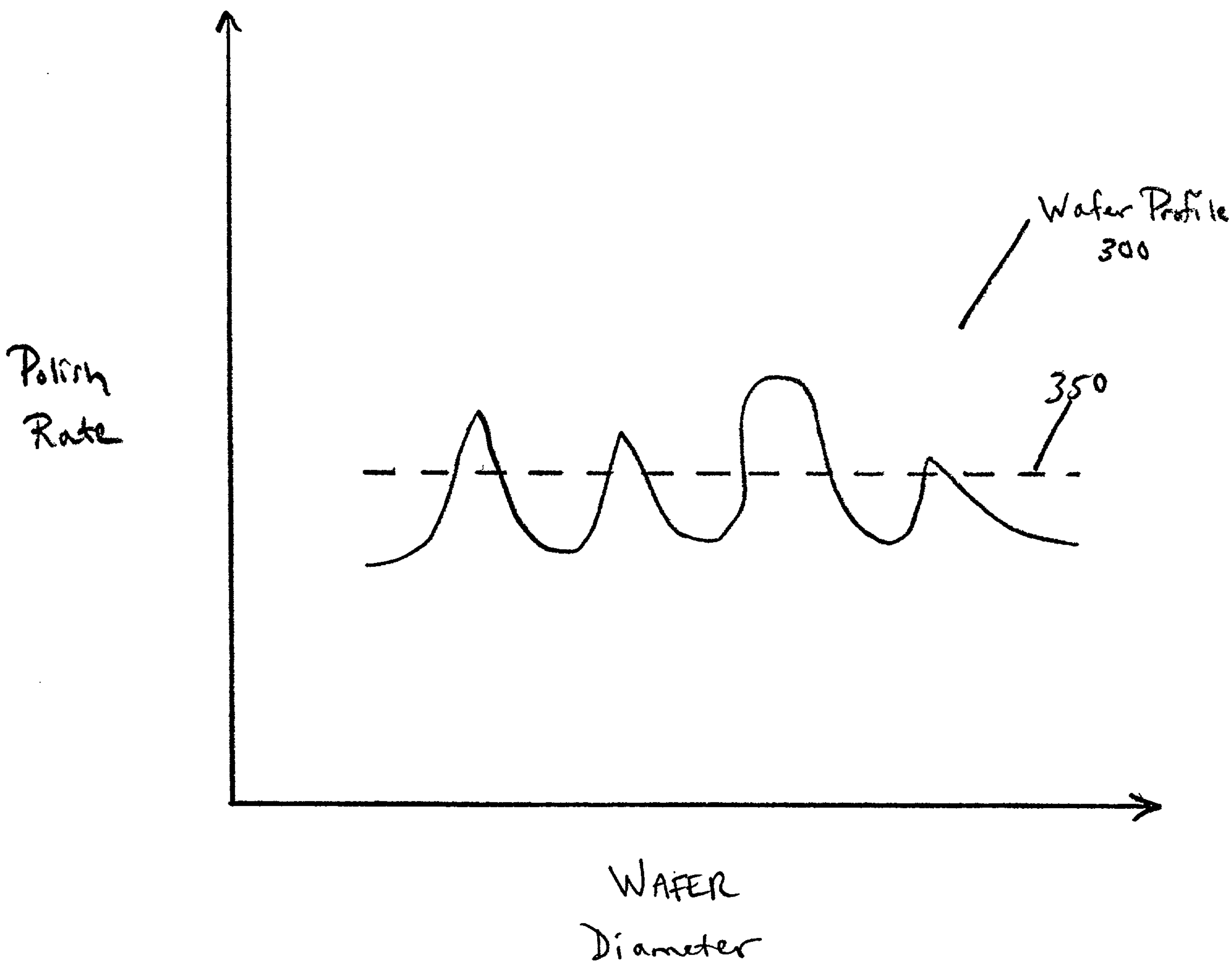

FIGURE 3

Figure 4A

Figure 4B

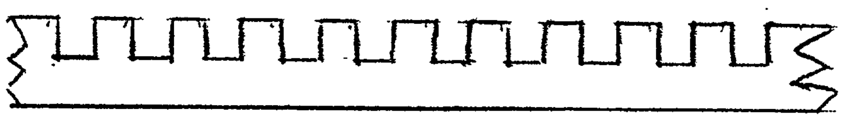

Figure 4C

Figure 5A

Fig 1

Figure 5B

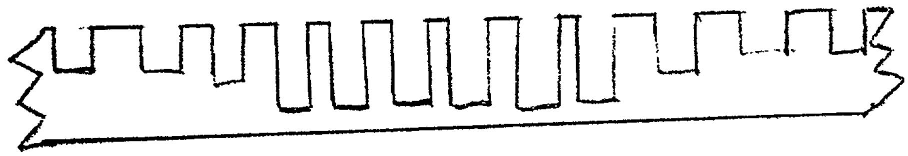

Figure 6

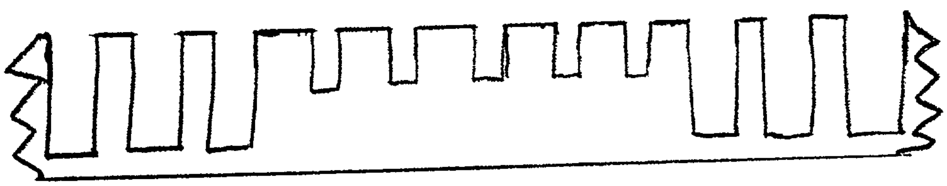

Fig. 2

Figure 7

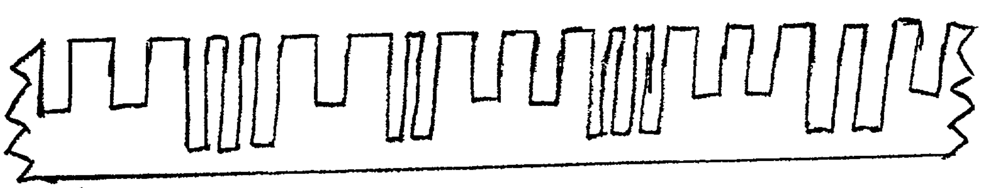

Fig 3

Attorney's Docket No.: 42390.P3955 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Polish Pad with Non-Uniform Groove Depth to Improve Wafer Polish Rate Uniformity

the specification of which

_____ is attached hereto.
__X__ was filed on December 23, 1997 as United States Application Number 08/997,293 or PCT International Application Number ______ and was amended on ______.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.